ABSTRACT OF THE DISCLOSURE

A chip resistor comprising a substrate having opposite parallel symmetrical first and second surfaces, a central longitudinal plane of symmetry, separate and spaced first and second resistive layers on the first and second surfaces. The resistive layers are electrically connected in parallel to each other and the first and second surfaces of the substrate are symmetrically located with respect to and equidistant from a central longitudinal plane. Thus, when electrical current passes through the resistive layers, a temperature distribution within the substrate will be substantially symmetrical about the central longitudinal plane of the substrate for eliminating thermal bending thereof. The splitting of the surge current between two resistive layers results in the lower temperature in each resistive layer when compared with the temperature in the single resistive layer of the prior art chip resistor loaded by the same current.